In the Claims:

Please cancel Claims 1-12.

13. (Original) A method of storing, in a latch circuit, information concerning a condition of a fuse; said latch circuit comprising a pair of inverter circuits, a first transistor, and a second transistor; said pair of inverter circuits being connected in anti-parallel with a common input terminal and a common output terminal; said first transistor having a first terminal coupled to said input terminal of said pair of inverter circuits, a further terminal coupled to a further terminal of said fuse, and a gate terminal coupled to a strobe line; and said second transistor having a first terminal coupled to a supply voltage, a further terminal coupled to said further terminal of said fuse and to said further terminal of said first transistor, and a gate terminal coupled to a pre-charge line; said method comprising:

supplying a first signal on said strobe line that activates said first transistor thereby setting said input terminal of said pair of inverter circuits at a first voltage state when said fuse is in a first condition and keeping a voltage state of said input terminal of said pair of inverter circuits unchanged when said fuse is in a second condition; and

supplying a second signal on said pre-charge line while said first signal is being supplied on said strobe line, said second signal activating said second transistor thereby keeping said input terminal of said pair of inverter circuits in said first voltage state when said fuse is in said first condition and setting said input terminal of said pair of inverter circuits at a second voltage state when said fuse is in said second condition.

14. (Original) The method of claim 13 wherein said fuse is in said first condition when said fuse is intact, and said fuse is in said second condition when said fuse is blown.

15. (Original) The method of claim 13 wherein said first signal is initiated by a change from a lower voltage to a higher voltage, and said first transistor is an n-channel transistor.

16. (Original) The method of claim 13 wherein said second signal is initiated by a change from a higher voltage to a lower voltage, and said second transistor is a p-channel transistor.

17. (Original) The method of claim 13 wherein said first voltage state comprises a lower voltage and said second voltage state comprises a higher voltage.

18. (Original) The method of claim 13 further comprising terminating said first signal and said second signal concurrently.

19. (Original) A method of correcting an error in information stored in a latch circuit concerning a condition of a fuse; said latch circuit comprising a pair of inverter circuits, a first transistor, and a second transistor; said pair of inverter circuits being connected in anti-parallel with a common input terminal and a common output terminal; said first transistor having a first terminal coupled to said input terminal of said pair of inverter circuits, a further terminal coupled to a further terminal of said fuse, and a gate terminal coupled to a strobe line; and said second transistor having a first terminal coupled to a supply voltage, a further terminal coupled to said further terminal of said fuse and to said further terminal of said first transistor, and a gate

terminal coupled to a pre-charge line; said method comprising:

supplying a first signal on said strobe line that activates said first transistor thereby setting said input terminal of said pair of inverter circuits at a first voltage state when said fuse is in a first condition and keeping a voltage state of said input terminal of said pair of inverter circuits unchanged when said fuse is in a second condition; and

supplying a second signal on said pre-charge line while said first signal is being supplied on said strobe line, said second signal activating said second transistor thereby keeping said input terminal of said pair of inverter circuits in said first voltage state when said fuse is in said first condition and setting said input terminal of said pair of inverter circuits at a second voltage state when said fuse is in said second condition.

20. (Original) The method of claim 19 wherein said fuse is in said first condition when said fuse is intact, and said fuse is in said second condition when said fuse is blown.

21. (Original) The method of claim 19 wherein said first signal is initiated by a change from a lower voltage to a higher voltage, and said first transistor is an n-channel transistor.

22. (Original) The method of claim 19 wherein said second signal is initiated by a change from a higher voltage to a lower voltage, and said second transistor is a p-channel transistor.

23. (Original) The method of claim 19 wherein said first voltage state comprises a lower voltage and said second voltage state comprises a higher voltage.

24. (Original) The method of claim 19 further comprising terminating said first signal and said second signal concurrently.

Please cancel Claims 25-32.

33. (Previously Presented) A latch circuit for reading, holding and outputting information concerning a condition of a fuse, said fuse having a first terminal coupled to a ground potential, said circuit comprising:

a pair of inverter circuits connected in an anti-parallel arrangement and with a common input terminal and a common output terminal;

a first transistor having a first terminal coupled to said input terminal of said pair of inverter circuits, a further terminal coupled to a further terminal of said fuse, and a gate terminal coupled to a first signal line; and

a second transistor having a first terminal coupled to a supply voltage, a further terminal coupled to said further terminal of said fuse and to said further terminal of said first transistor, and a gate terminal coupled to a second signal line;

said first transistor, when activated by a first signal delivered by said first signal line, setting said input terminal of said pair of inverter circuits at a first voltage when said fuse is in a first condition and keeping a voltage state of said input terminal of said pair of inverter circuits unchanged when said fuse is in a second condition;

said second transistor, when activated by a second signal delivered by said second signal line while said first signal is being delivered by said first signal line, keeping said input terminal of said pair of inverter circuits at said first voltage when said fuse is in said first condition and

setting said input terminal of said pair of inverter circuits at a second voltage when said fuse is in said second condition.

34. (Original) The latch circuit of claim 33 wherein said fuse is in said first condition when said fuse is intact, and said fuse is in said second condition when said fuse is blown.

35. (Original) The latch circuit of claim 33 wherein said first state comprises a lower voltage and said second state comprises a higher voltage.

36. (Original) The latch circuit of claim 33 wherein said first signal line comprises a strobe signal line.

37. (Original) The latch circuit of claim 33 wherein said second signal line comprises a pre-charge signal line.

38. (New) The latch circuit of claim 33 wherein said first transistor is an n-channel transistor.

39. (New) The latch circuit of claim 33 wherein said second transistor is a p-channel transistor.

40. (New) A latch circuit for reading, holding and outputting information concerning a condition of a fuse, said fuse having a first terminal coupled to a ground potential, said circuit comprising:

a pair of inverter circuits connected in an anti-parallel arrangement and with a common input terminal and a common output terminal;

a first transistor having a first terminal coupled to said input terminal of said pair of inverter circuits, a further terminal coupled to a further terminal of said fuse, and a gate terminal coupled to a first signal line; and

a second transistor having a first terminal coupled to a supply voltage, a further terminal coupled to said further terminal of said fuse and to said further terminal of said first transistor, and a gate terminal coupled to a second signal line.

41. (New) The latch circuit of claim 40,

wherein said first transistor, when activated by a first signal delivered by said first signal line, setting said input terminal of said pair of inverter circuits at a first voltage when said fuse is in a first condition and keeping a voltage state of said input terminal of said pair of inverter circuits unchanged when said fuse is in a second condition,

wherein said second transistor, when activated by a second signal delivered by said second signal line while said first signal is being delivered by said first signal line, keeping said input terminal of said pair of inverter circuits at said first voltage when said fuse is in said first condition and setting said input terminal of said pair of inverter circuits at a second voltage when said fuse is in said second condition,

wherein said fuse is in said first condition when said fuse is intact, and said fuse is in said second condition when said fuse is blown, and

wherein said first state comprises a lower voltage and said second state comprises a higher voltage.

42. (New) The latch circuit of claim 40 wherein said first signal line comprises a strobe signal line, and wherein said second signal line comprises a pre-charge signal line.

43. (New) The latch circuit of claim 40 wherein said first transistor is an n-channel transistor, and wherein said second transistor is a p-channel transistor.

44. (New) A fuse latch circuit comprising:

a fuse having a first fuse terminal and a second fuse terminal,

said first fuse terminal being electrically coupled to a first node, and

said second fuse terminal being electrically coupled to a ground line;

a p-channel transistor having a gate terminal, a first terminal, and a second terminal,

said gate terminal of said p-channel transistor being electrically coupled to a pre-charge line,

said first terminal of said p-channel transistor being electrically coupled to a supply voltage line, and

said second terminal of said p-channel transistor being electrically coupled to said first node;

a pair of inverter circuits connected in an anti-parallel arrangement and having a common input terminal and a common output terminal;

an n-channel transistor having a gate terminal, a first terminal, and a second terminal,

said gate terminal of said n-channel transistor being electrically coupled to a readout strobe line,

said first terminal of said n-channel transistor being electrically coupled to said common input terminal of said pair of inverter circuits, and

said second terminal of said n-channel transistor being electrically coupled to said first node.